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AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1-2. Cancelled

3. (Currently Amended) A ~~digital-control-type~~ digital-control type clock data recovery circuit comprising:

a phase comparator comparing a phase of input data with a phase of a data recovery clock signal generated internally, outputting a DOWN signal to delay said data recovery clock signal when an ~~rising~~ edge of said input data is detected during a first term ~~after~~ before said data recovery clock signal and outputting an UP signal to set forward the phase of said data recovery clock signal when an ~~falling~~ edge of said input data is detected during a second term ~~before~~ after said data recovery clock signal;

a multistage register circuit storing onset of said DOWN signal and onset of said UP signal at each of comparing opportunities during a phase detection period corresponding to a plurality of cycles of said data recovery clock signal, generating an OUT DOWN signal if at least one DOWN signal is stored at an end of the phase detection period and generating an OUT UP signal if at least one UP signal is stored

at the end of the phase detection period~~a counter for effectuating said UP signal when said UP signal is repeatedly generated and effectuating said DOWN signal when said DOWN signal is repeatedly generated~~; and

a clock-phase generation unit generating said data recovery clock signal and shifting the phase of said data recovery clock signal on the basis of the ~~effectuated~~ OUT UP signal and the ~~effectuated~~ OUT DOWN signal output from said ~~counter~~ multistage register circuit so as to separate edges of said data recovery clock signal away from edges of said input data by a predetermined time gap;

wherein said input data is taken in with a timing of said data recovery clock signal.

4. Cancelled.

5. (Currently Amended) A digital-control type clock data recovery circuit according to claim 3, wherein said clock-phase generation unit includes a phase variable delay circuit for generating N clock signals with phases different from each other on the basis of a reference clock signal, and for selecting one of said N clock signals in accordance with a phase selection signal, where N is a finite number, and a cyclic clock phase pointer setting and changing said phase selection signal in accordance with the ~~effectuated~~ OUT UP signal and the ~~effectuated~~ OUT DOWN signal.

6. Cancelled.

7. (Previously Presented) A digital-control type clock data recovery circuit according to claim 5, wherein said phase variable-delay circuit comprises a buffer, a composition circuit, an N-1 selector and a CMOS level conversion circuit, and said buffer, said composition circuit, said N-1 selector and said CMOS level conversion circuit are each designed as a small-amplitude differential circuit.

8. (Previously Presented) A digital-control type clock data recovery circuit according to claim 7, wherein, by executing control to turn on 2 of N selector control signals supplied to each 2 adjacent pins of said N-1 selector at the same time, said N-1 selector is capable of generating a middle phase between first and second phases and, hence, obtaining N × 2 phases from N input phases.

9. (Canceled).

10. (Previously Presented) A digital-control type clock data recovery circuit comprising:

comparing circuitry containing a function to track a wander of input data by comparing a position of an edge of said input data with a position of an edge of a clock signal,

wherein said function to track a wander of input data by comparing a position

of an edge of said input data with a position of an edge of a clock signal is executed under a condition expressed by a relation given as follows:

$$B \times \sin(2\pi \times Ta/Tw) < T/N$$

where symbol B denotes a maximum phase change of said input data over a period of time, symbol Ta denotes a loop delay, which is a period of time between an output operation carried out by a counter and a first phase comparison, symbol Tw denotes a phase deviation period, symbol T denotes a clock period, symbol N denotes the number of phase divisions, where N is a finite number, and T/N denotes a difference between 2 adjacent phases determined by said number of phase divisions N.

11-12. (Canceled).

13. (Previously Presented) A digital-control type clock data recovery circuit comprising:

a control circuit for comparing a position of an edge of data with a position of an edge of a data recovery clock signal to execute control for placing said edge of said data recovery clock signal in an eye narrowed by high-frequency phase deviations (jitters) of said data,

wherein said data is taken in with a timing of said edge of said data recovery clock signal, and

wherein said control circuit compares said position of said edge of said data recovery clock signal with said position of said edge of said data at a first

predetermined frequency and changes a phase of said data recovery clock signal at a second predetermined frequency not exceeding said first predetermined frequency.